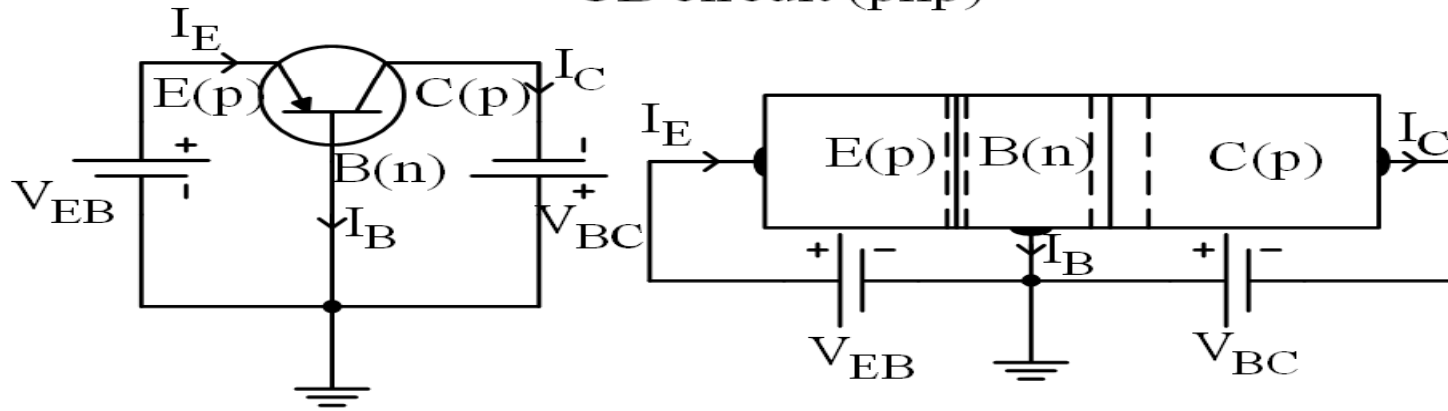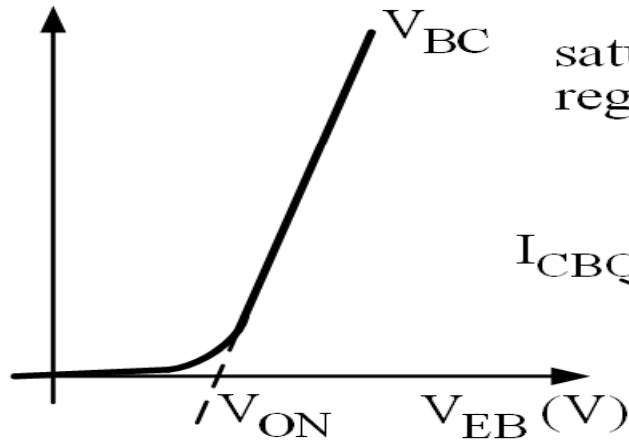# CLASS 20

BJT PARAMETERS AND BIASING
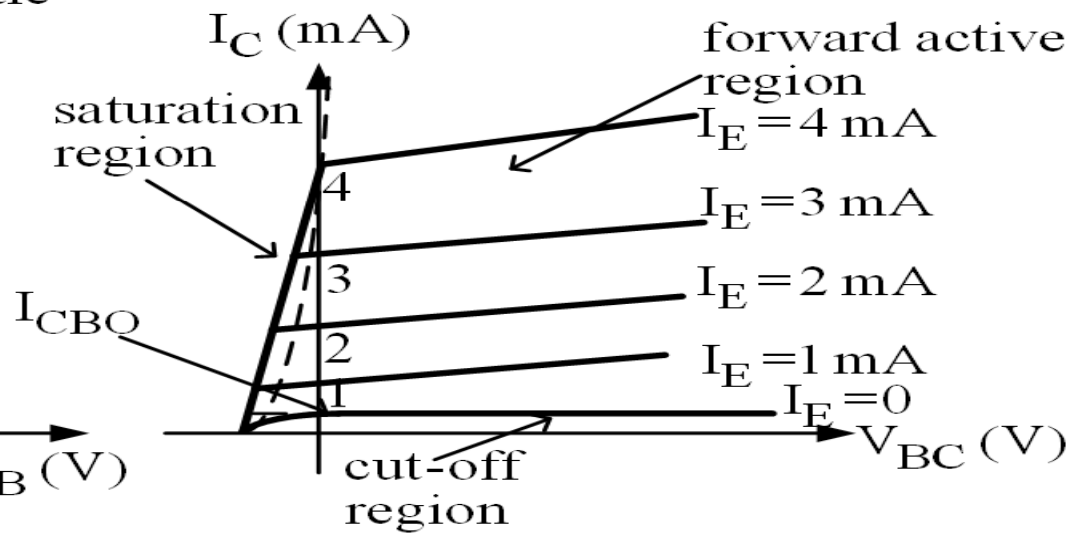
CB circuit (pnp)

input characteristic

I_E (mA)

V_{BC}

V_{ON} V_{EB} (V)

output characteristic

I_C (mA)

forward active region

$I_E = 4$ mA

saturation region

$I_E = 3$ mA

$I_E = 2$ mA

I_{CBO}

$I_E = 1$ mA

$I_E = 0$

V_{BC} (V)

cut-off region

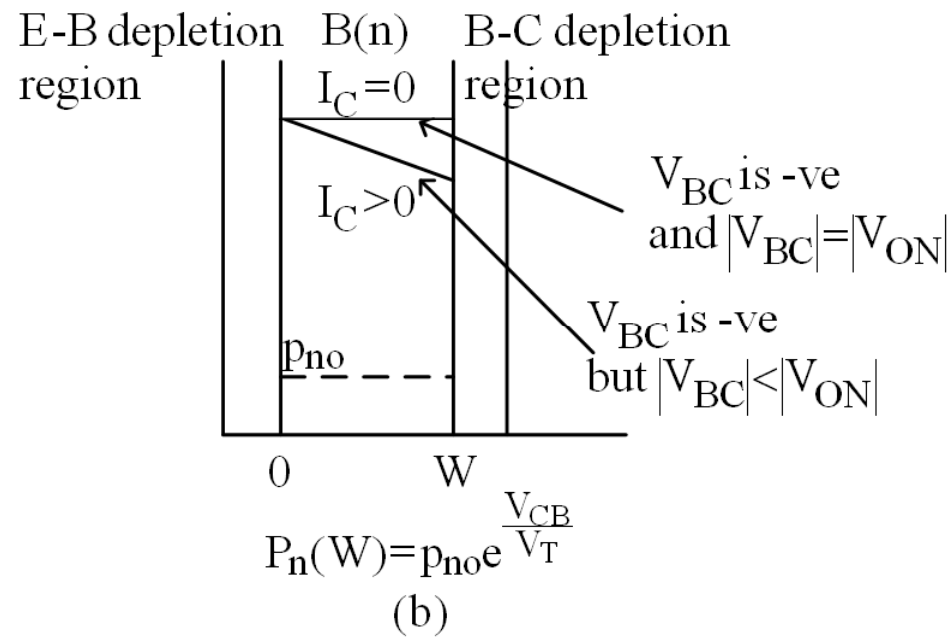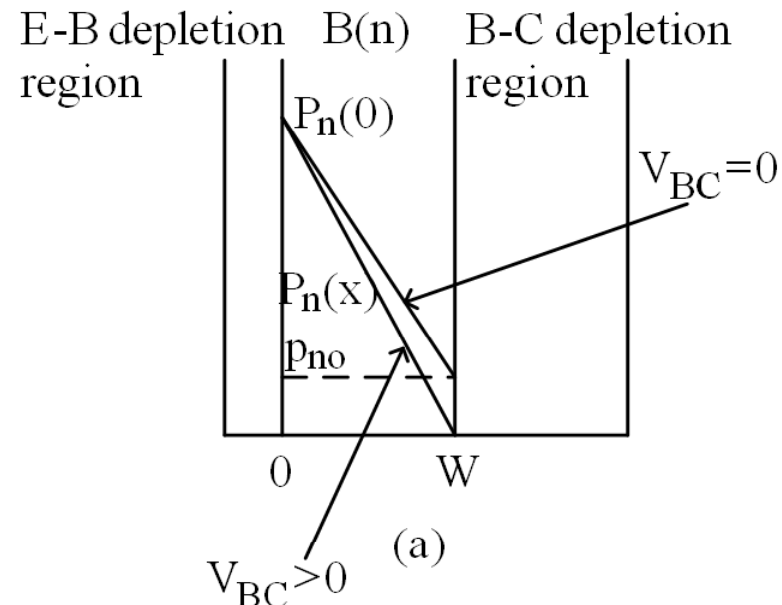In the active region, $I_C \approx I_E$ and is independent of V_{BC}. $I_C \approx \alpha_o I_E$

Observations

- $V_{BC}\uparrow I_C\uparrow$ because when $V_{BC}\uparrow$, the B-C junction becomes more rb. The width of the effective B region (outside depletion) becomes smaller. Recombinations $\downarrow$. Hence, $I_C\uparrow$.

- At a fixed V_{BC}, if $I_E\uparrow I_C\uparrow$. As $I_C = \alpha_o I_E$ and $\alpha_o \approx 1$, $I_C \approx I_E$. Thus, $I_E\uparrow I_C\uparrow$.

- If $V_{BC} = 0$, there still exists a depletion region at the B-C junction. Fixed –ve ions in the depletion region of the C can still manage to attract the holes from B to cross the B-C junction and enter C. I_C exists. If the V_{BC} becomes –ve (i.e. V_C is more +ve than V_B), the width of the depletion region$\downarrow$ and $I_C \downarrow$. When $V_{CB} = V_{ON}$, the depletion region's width ≈ 0. At this time, the B-C junction becomes fb and $I_C = 0$.

output characteristic

input characteristic
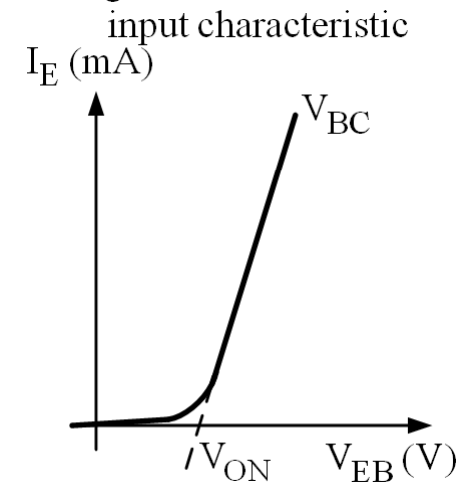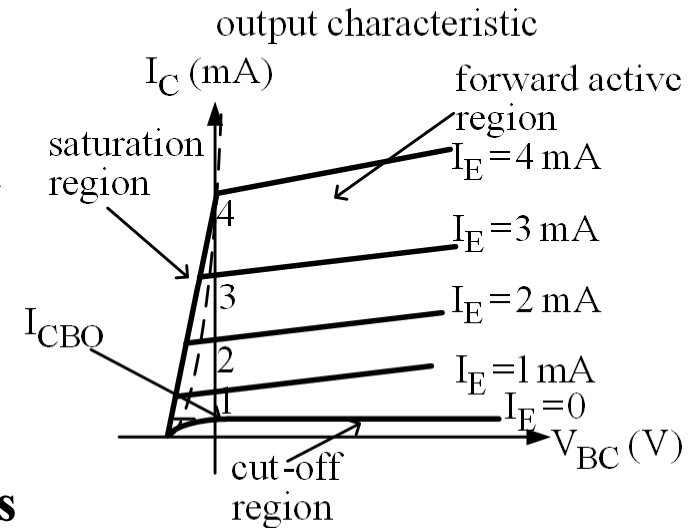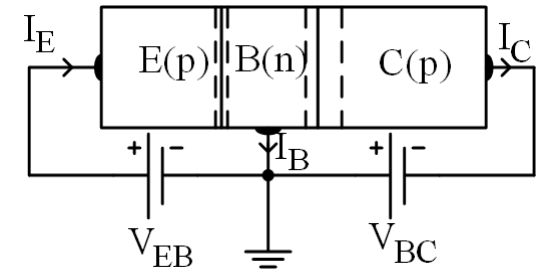
Distribution of minority carriers in B for a pnp transistor.

(a) Active mode for $V_{BC} \geq 0$.

(b) Saturation mode with both E-B and B-C junctions fb.

I_E E(p) | B(n) | C(p) I_C

I_B

V_{EB} V_{BC}

output characteristic

I_C (mA)

saturation region

forward active region

$I_E = 4\,mA$

$I_E = 3\,mA$

$I_E = 2\,mA$

I_{CBO}

$I_E = 1\,mA$

$I_E = 0$

V_{BC} (V)

cut-off region

E-B depletion region   B(n)   B-C depletion region

$P_n(0)$

$V_{BC}=0$

$P_n(x)$

p_{no}

0   W

$V_{BC} > 0$ (a)

E-B depletion region   B(n)   B-C depletion region

$I_C = 0$

$I_C > 0$

V_{BC} is -ve and $|V_{BC}|=|V_{ON}|$

V_{BC} is -ve but $|V_{BC}|<|V_{ON}|$

p_{no}

0   W

V_{CB}

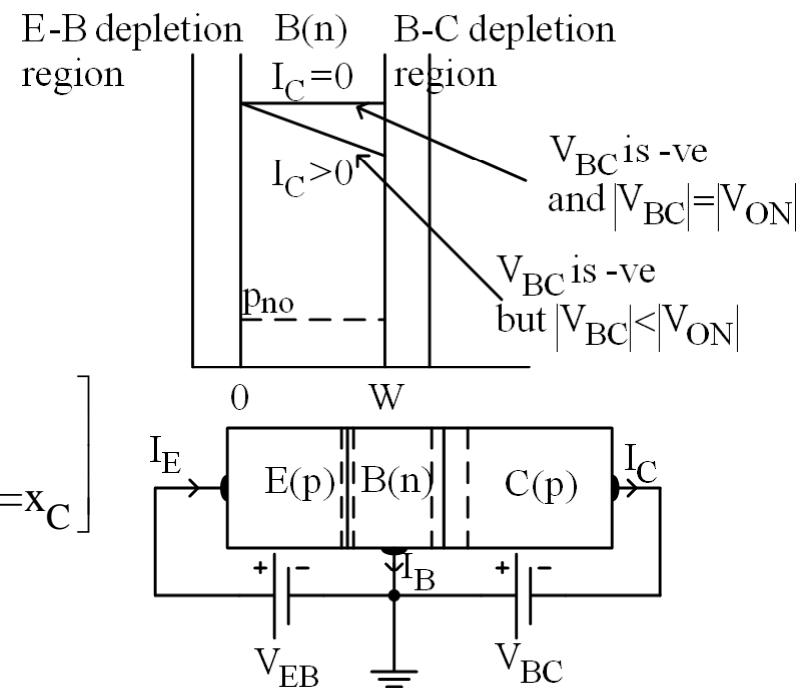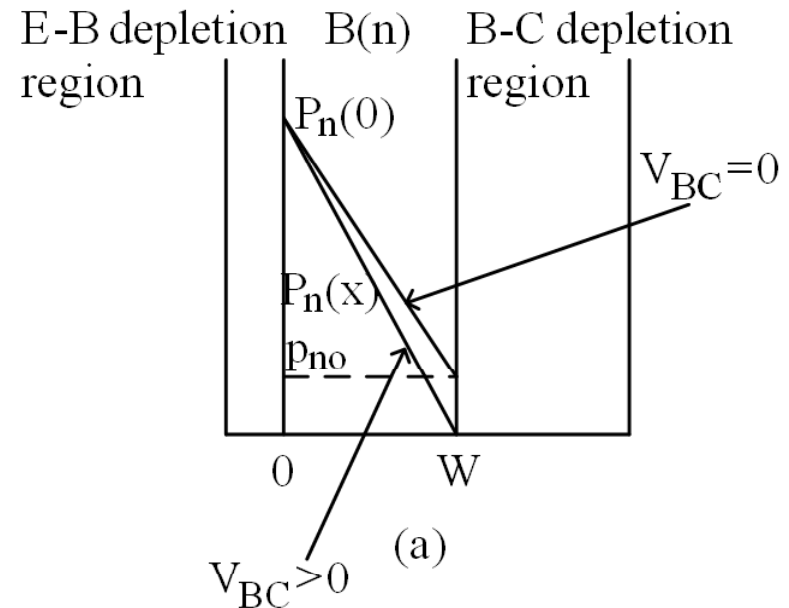$P_n(W)=p_{no}e^{\frac{V_{CB}}{V_T}}$

(b)
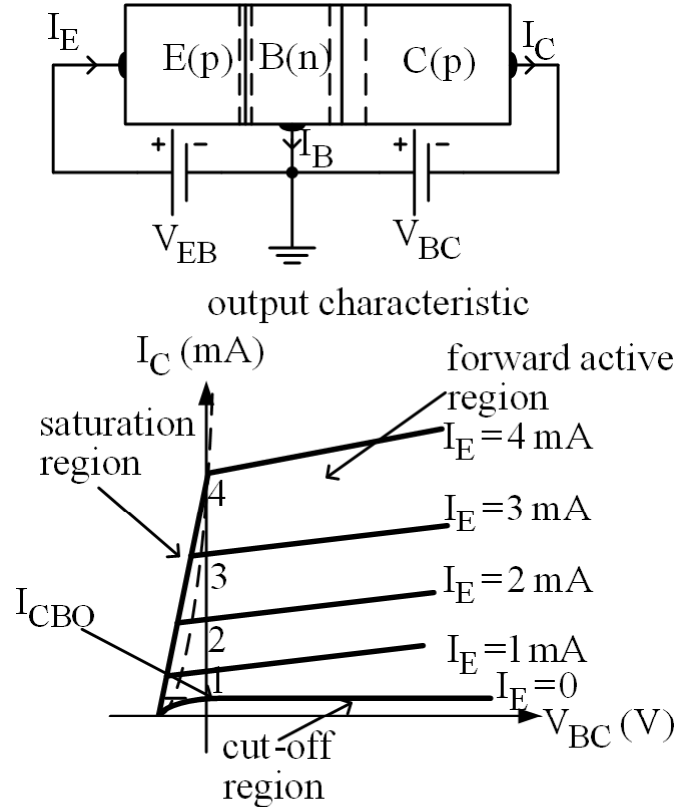
Observations

- Since the difference in the slope is not large when $V_{BC} > 0$ and $V_{BC} = 0$, I_C does not change much.

- $I_C = 0$ when one small forward voltage is supplied across the B-C junction ($V_{CB} \approx 1$ V for Silicon). Under this condition, the transistor is in the saturation region.

- The fb supplied to the B-C junction will increase the hole density at x=W until it reaches a value equals to the hole density at x=0. This means that the hole gradient at x=w and consequently I_C will reduced to 0.

$$I_{Cp} = A\left[-qD_p \frac{dp_n}{dx}\Big|_{x=W}\right] , \quad I_{Cn} = A\left[qD_C \frac{dn_C}{dx}\Big|_{x=x_C}\right]$$

$$\approx \frac{qAD_p p_{no}}{W} e^{(qV_{EB})/kT} \qquad = \frac{qAD_C n_{Co}}{L_C}$$

E-B depletion region   B(n)   B-C depletion region

$P_n(0)$

$V_{BC}=0$

$P_n(x)$

p_{no}

0   W

$V_{BC}>0$

(a)

E-B depletion region   B(n)   B-C depletion region

$I_C=0$

$I_C>0$

V_{BC} is -ve and $|V_{BC}|=|V_{ON}|$

V_{BC} is -ve but $|V_{BC}|<|V_{ON}|$

p_{no}

0   W

I_E E(p) B(n)   C(p) I_C

I_B

V_{EB} V_{BC}

Important observations:

$$I_E = I_B + I_C$$

For the CB,

$$I_C = \alpha_o I_E + I_{CBO}$$

where I_{CBO} is the C-B current when E is open ($I_E = 0$) and it is a minority carrier current.

$$I_C = \alpha_o (I_B + I_C) + I_{CBO}$$

$$I_C (1 - \alpha_o) = \alpha_o I_B + I_{CBO}$$

$$I_C = (\alpha_o I_B + I_{CBO}) / (1 - \alpha_o) = [\alpha_o I_B / (1 - \alpha_o)] + [I_{CBO} / (1 - \alpha_o)]$$
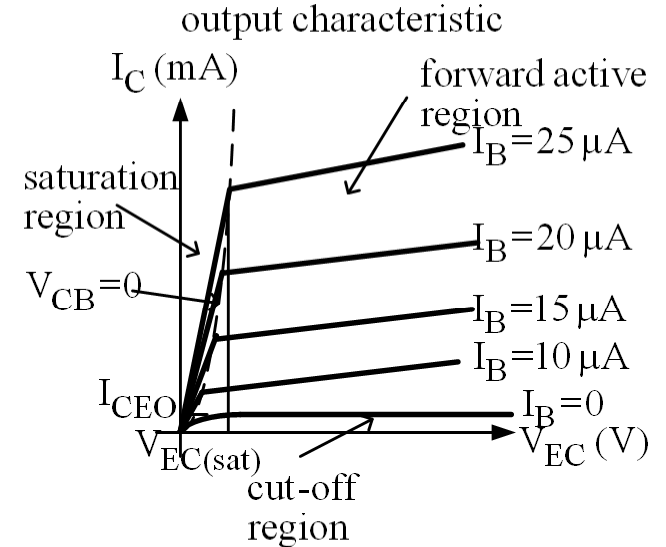
$$\alpha_o / (1 - \alpha_o) = \beta_{DC} = \text{CE DC current gain}$$

$$\beta_{DC} = \Delta I_C / \Delta I_B$$

$$I_{CEO} = I_{CBO} / (1 - \alpha_o)$$

where I_{CEO} is the leakage current when B is open ($I_B = 0$) and it is a minority carrier current.

$$I_C = \beta_{DC} I_B + I_{CEO}$$

output characteristic

I_C (mA)

forward active region

$I_B = 25\,\mu A$

saturation region

$I_B = 20\,\mu A$

$V_{CB} = 0$

$I_B = 15\,\mu A$

$I_B = 10\,\mu A$

I_{CEO}

$I_B = 0$

V_{EC} (V)

$V_{EC(sat)}$

cut-off region

$I_{CEO} = I_{CBO} / (1 - \alpha_o) = I_{CBO} / \{1 - [\beta_{DC} /(1 + \beta_{DC})]\}$

$I_{CEO} = I_{CBO} (1 + \beta_{DC}) / \{(1 + \beta_{DC}) - \beta_{DC} \} = I_{CBO} (1 + \beta_{DC})$

$\beta_{DC} = \alpha_o / (1 - \alpha_o);$ **this expression shows that $\beta_{DC} > 1$**

$\alpha_o = \beta_{DC} (1 - \alpha_o) = \beta_{DC} - \beta_{DC} \alpha_o$

$\alpha_o (1 + \beta_{DC}) = \beta_{DC}$

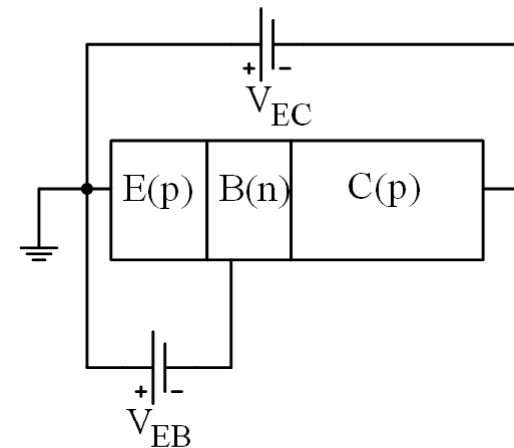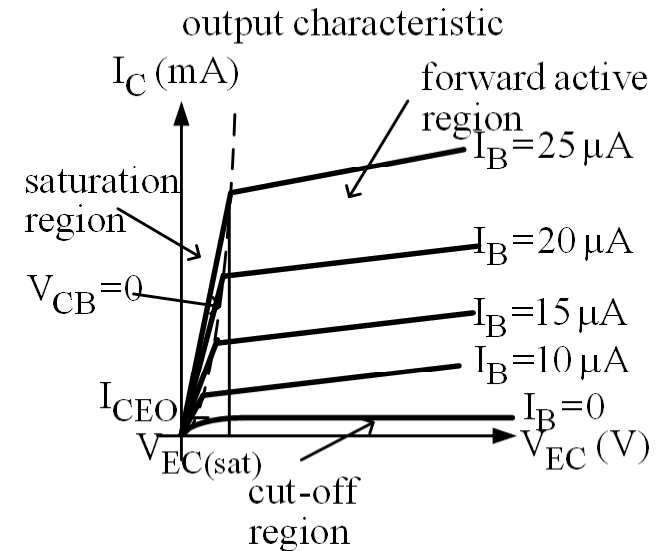$\boxed{\alpha_o = \beta_{DC} /(1 + \beta_{DC})};$ **this expression shows that $\alpha_o < 1$**

$\alpha_o \approx 1.$ **Thus, $\beta_{DC} \gg 1.$**

If $\alpha_o = 0.99, \beta_{DC} = 0.99 / (1 - 0.99) = 99.$

If $\alpha_o = 0.998, \beta_{DC} = 0.998 / (1 - 0.998) = 499.$

These results show that a small change in I_B will cause a large difference in I_C .

From the output characteristics of the CE, there is still output current, I_C, flowing although $I_B = 0$ and this is the I_{CEO} which is the leakage current when $I_B=0$.

output characteristic

I_C (mA)

forward active region

$I_B=25\,\mu A$

saturation region

$I_B=20\,\mu A$

$V_{CB}=0$

$I_B=15\,\mu A$

$I_B=10\,\mu A$

I_{CEO}

$I_B=0$

$V_{EC(sat)}$

V_{EC} (V)

cut-off region

V_{EC}

E(p) | B(n) | C(p)

V_{EB}

BIASING

- **The BJT must be biased in order to operate it as an amplifier.**
- **A DC operating point must be set so that the signal at the input terminal can be amplified and reproduced without any distortion at the output terminal.**
- **For the CE amplifier, the DC operating point is I_C and V_{CE}. The operating point must be in the active region in order for the BJT to operate as an amplifier.**
- **The DC operating point is known as the quiescent (Q) point. For the CE amplifier, the Q point is I_{CQ} and V_{CEQ}.**
- **With the correct biasing, the circuit need not be changed or redesign when another transistor from the same type is substituted or when the temperature changes. Hence, a biasing circuit needs to be stable.**

To determine the operating point:

- The DC load line is drawn on the output characteristic to determine the operating current and voltage of the circuit. The intersection of the load line with the I and V axis depends on the circuit's schematic.

- A DC biasing point / quiescent (Q) point is determined from the load line in the active region. The Q point is a point on the load line that represents the current and voltage at the output of a transistor when there is no AC signal. The stability of a biasing point is influenced by the change in the parameters (as an example: β_{DC}) when the transistor is replaced by another transistor of the same type or by the change in temperature.

From Floyd, Electronic Devices, Sixth Edition.

2N3903
2N3904

3 Collector

2 Base

1 Emitter

General-Purpose Transistors

NPN Silicon

Maximum Ratings

Rating	Symbol	Value	Unit
Collector-Emitter voltage	V_{CEO}	40	V dc
Collector-Base voltage	V_{CBO}	60	V dc
Emitter-Base voltage	V_{EBO}	6.0	V dc
Collector current — continuous	I_C	200	mA dc
Total device dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total device dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and storage junction Temperature range	T_J, T_{stg}	−55 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, junction to case	$R_{\theta JC}$	83.3	°C/W
Thermal resistance, junction to ambient	$R_{\theta JA}$	200	°C/W
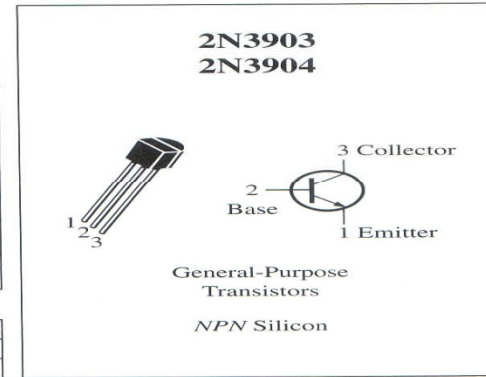
Electrical Characteristics ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF Characteristics					
Collector-Emitter breakdown voltage ($I_C = 1.0$ mA dc, $I_B = 0$)		$V_{(BR)CEO}$	40	—	V dc
Collector-Base breakdown voltage ($I_C = 10$ μA dc, $I_E = 0$)		$V_{(BR)CBO}$	60	—	V dc
Emitter-Base breakdown voltage ($I_E = 10$ μA dc, $I_C = 0$)		$V_{(BR)EBO}$	6.0	—	V dc
Base cutoff current ($V_{CE} = 30$ V dc, $V_{EB} = 3.0$ V dc)		I_{BL}	—	50	nA dc
Collector cutoff current ($V_{CE} = 30$ V dc, $V_{EB} = 3.0$ V dc)		I_{CEX}	—	50	nA dc
ON Characteristics					
DC current gain ($I_C = 0.1$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904	h_{FE}	20 40	— —	—
($I_C = 1.0$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		35 70	— —	
($I_C = 10$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		50 100	150 300	
($I_C = 50$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		30 60	— —	
($I_C = 100$ mA dc, $V_{CE} = 1.0$ V dc)	2N3903 2N3904		15 30	— —	
Collector-Emitter saturation voltage ($I_C = 10$ mA dc, $I_B = 1.0$ mA dc) ($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)		$V_{CE(sat)}$	— —	0.2 0.3	V dc
Base-Emitter saturation voltage ($I_C = 10$ mA dc, $I_B = 1.0$ mA dc) ($I_C = 50$ mA dc, $I_B = 5.0$ mA dc)		$V_{BE(sat)}$	0.65 —	0.85 0.95	V dc

▲ **FIGURE 4–19**

Partial transistor data sheet.

PARAMETERS THAT CAN CHANGE THE Q-POINT

- The DC current gain of the CE, β_{DC} or h_{FE} , for one type of transistor is typically available in a large range, h_{FE} = 50 to 300. The large range of β_{DC} or h_{FE} influences the transistor's biasing as

- $I_C = \beta_{DC} I_B$ (if the leakage current is neglected).

  If I_B is fixed and β_{DC} is varied, I_C will also change. I_{CQ} and V_{CEQ} will change, i.e. the operating point changes.

  The transistor might not be operating in the active region.

- Temperature can also change the operating point as the temperature changes the number of minority carriers. This can be seen from the expressions:

  $I_C = \beta_{DC} I_B + I_{CEO} = \alpha_o I_E + I_{CBO}$

  where the I_{CEO} and I_{CBO} are the minority carrier currents.
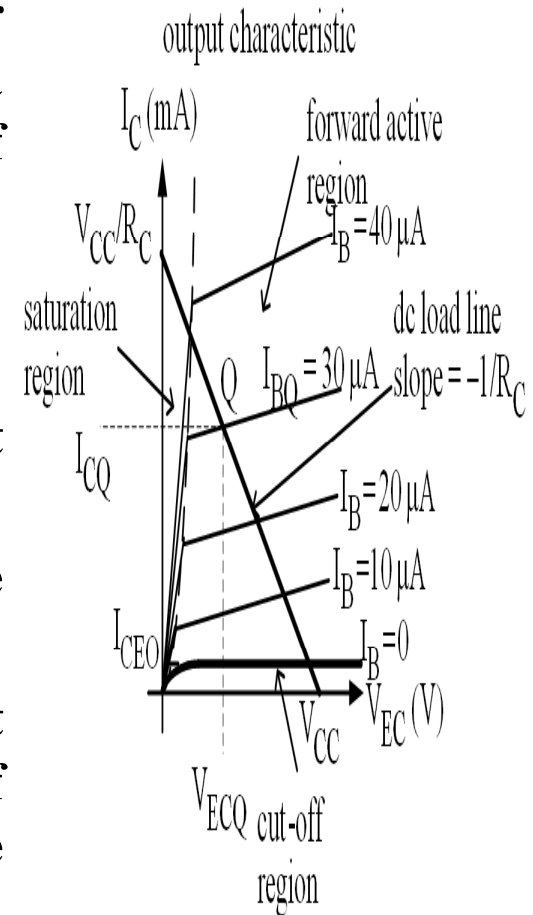
- **The dc load line can be determined by analyzing the transistor circuit. The transistor load line is linear and is in the form y = mx +c. By looking at the output characteristic of the CE, y = I_C , m = slope of the load line, x = V_{EC} and c = intersection of the load line with the I_C axis. The load line intersects the V_{EC} axis at I_C =0.**

- **When I_{BQ} is known, the value of I_{CQ} and V_{ECQ} can be determined by the intersection of the dc load line with the I_{BQ} curve.**

output characteristic

I_C (mA)

V_{CC}/R_C

forward active region

I_B=40 µA

saturation region

dc load line

Q I_{BQ}=30 µA   slope = –1/R_C

I_{CQ}

I_B=20 µA

I_B=10 µA

I_B=0

I_{CEO}

V_{CC} V_{EC} (V)

V_{ECQ} cut-off region
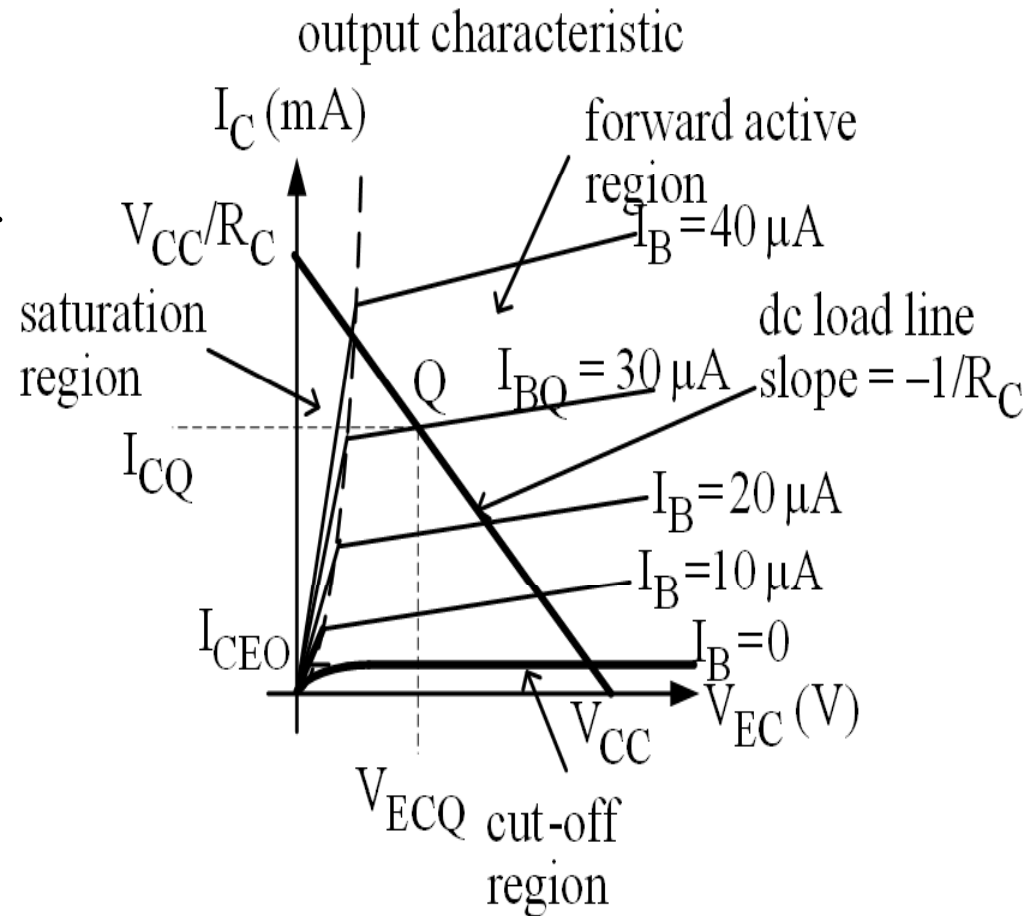
$$V_{EC} + I_C R_C - V_{CC} = 0$$
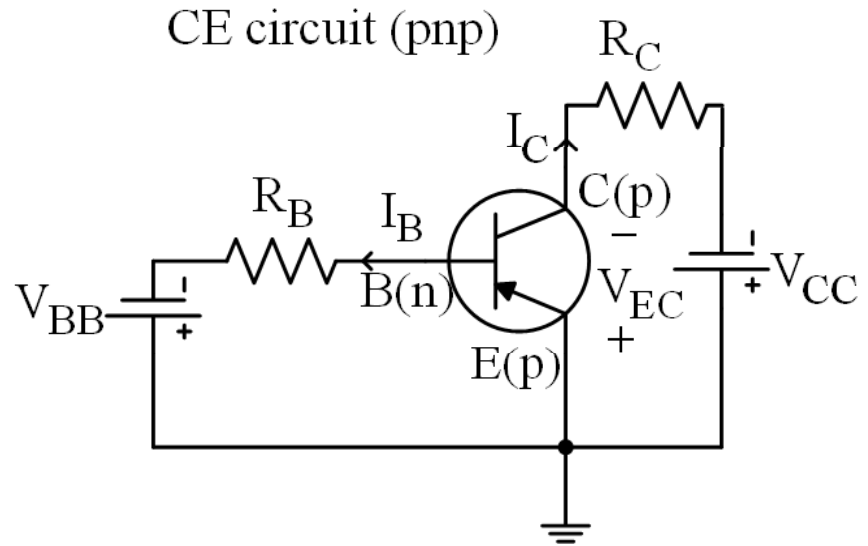
$$y = mx + c$$

$$y = I_C, \; x = V_{EC}$$

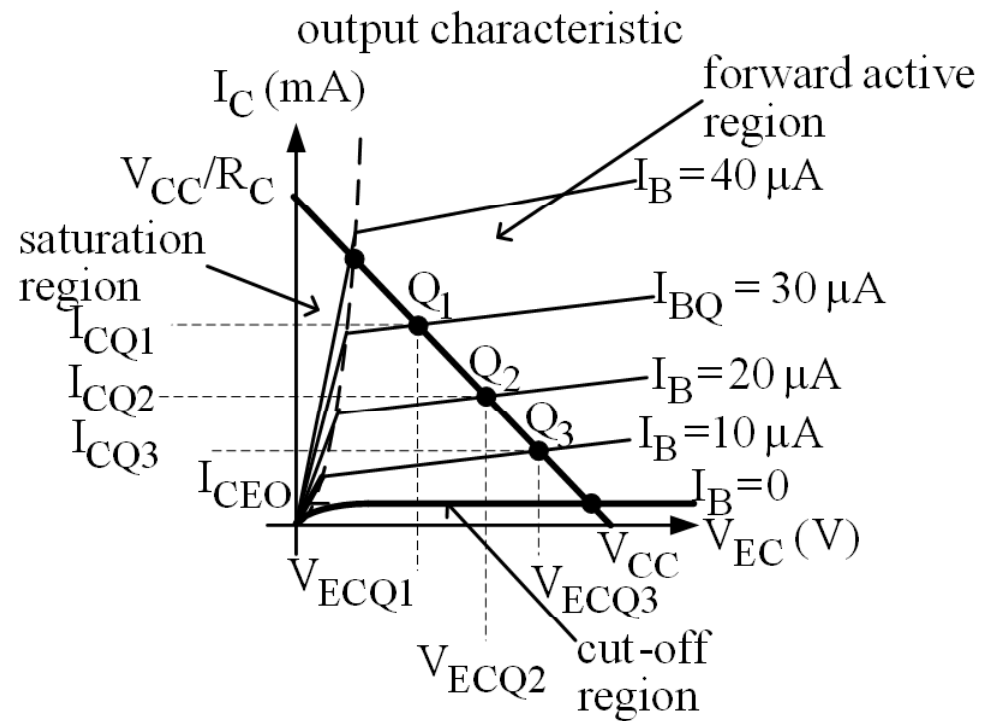$$I_C = -V_{EC} / R_C + V_{CC} / R_C$$

$$m = -1 / R_C, \; c = V_{CC} / R_C$$

When $I_C = 0$, $V_{EC} = V_{CC}$.

When $V_{EC} = 0$, $I_C = V_{CC} / R_C$.

CE circuit (pnp)
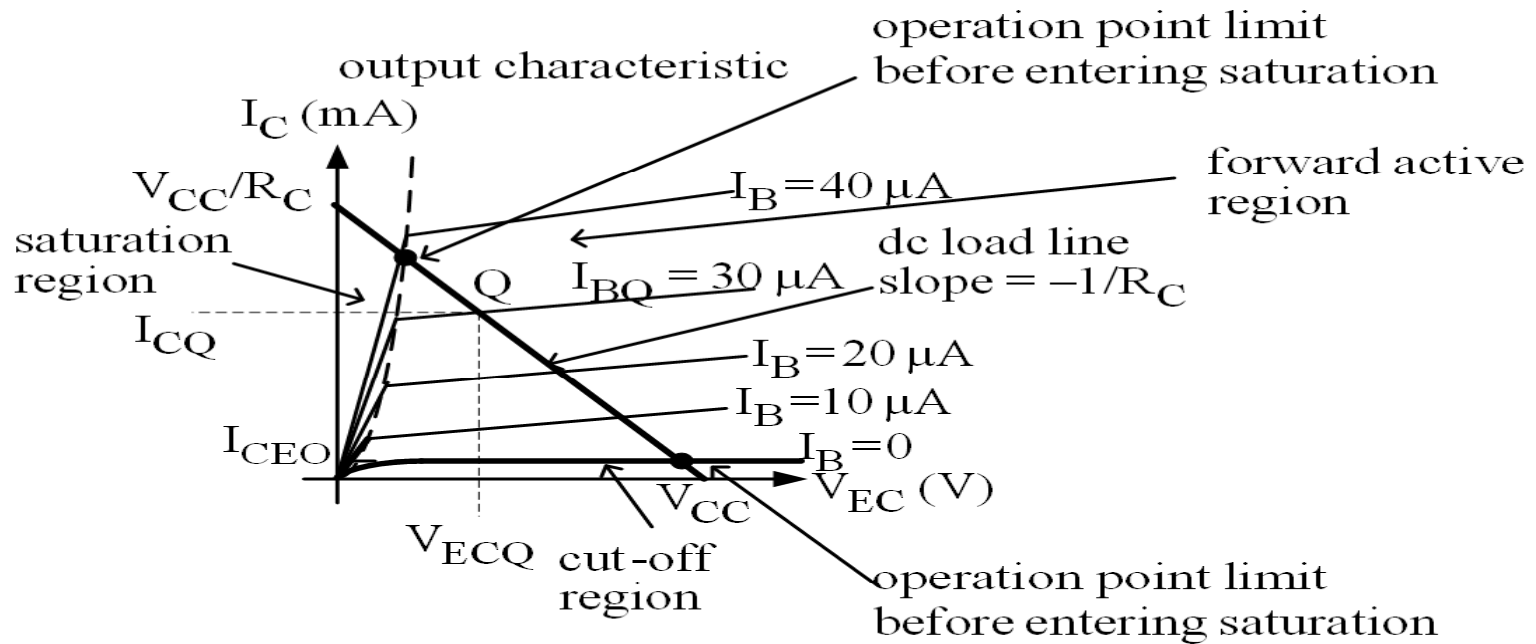
- **If the quiescent B current is I_{BQ}, then the operation point is Q_1 with output C current, I_{CQ1}, and E-C voltage, V_{CEQ1}.**

- **If the quiescent B current is 20 μA, then the operation point is Q_2 with output C current, I_{CQ2}, and E-C voltage, V_{CEQ2}.**

- **If the quiescent B current is 10 μA, then the operation point is Q_3 with output C current, I_{CQ3}, and E-C voltage, V_{CEQ3}.**

output characteristic

forward active region

I_C (mA)

V_{CC}/R_C

$I_B = 40\,\mu A$

saturation region

Q_1

$I_{BQ} = 30\,\mu A$

I_{CQ1}

Q_2

$I_B = 20\,\mu A$

I_{CQ2}

Q_3

$I_B = 10\,\mu A$

I_{CQ3}

I_{CEO}

$I_B = 0$

V_{ECQ1}

V_{CC}

V_{EC} (V)

V_{ECQ3}

V_{ECQ2}

cut-off region

If inaccurate Q is chosen:

- Transistor can be driven into saturation region (if Q is too close to the saturation region)
- Transistor can be driven into cut-off region (if Q is too close to the cut-off region)
- Transistor can be driven into both saturation and cut-off region (the Q point might be at the centre but the signal is too large)

  The result is a distorted signal at the output. This defeats the purpose of using the amplifier which is to have an amplified replica of the input signal at the output.

From Floyd, Electronic Devices, Sixth Edition.
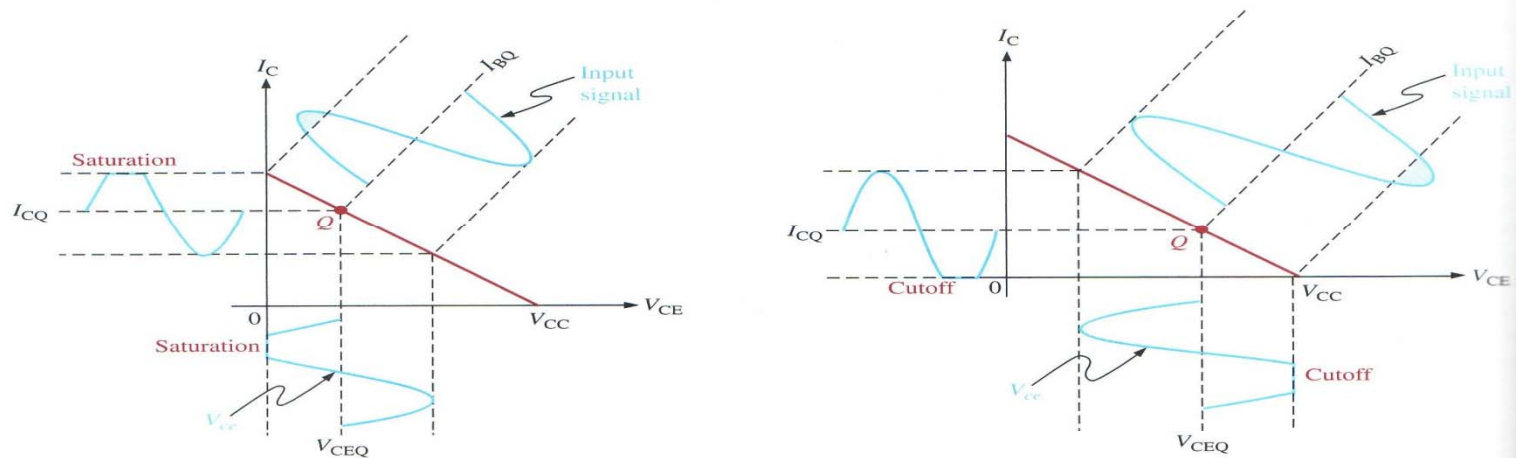
(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.
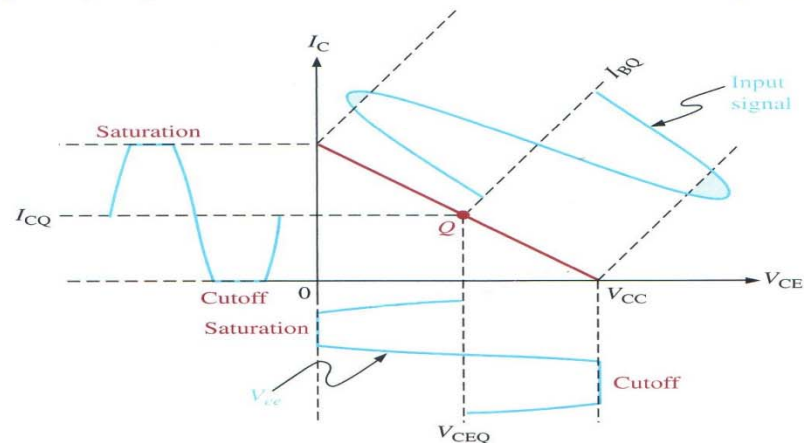
(c) Transistor is driven into both saturation and cutoff because the input signal is too large.
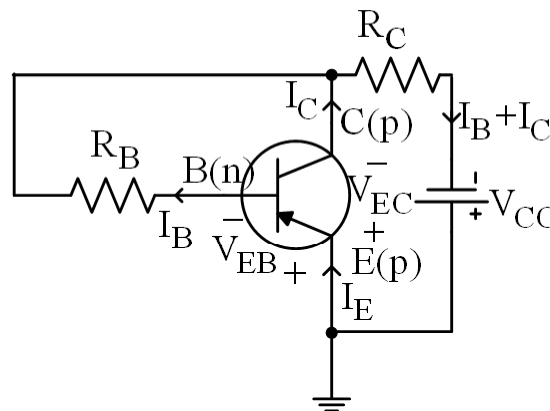
▲ FIGURE 5–6

Graphical load line illustration of a transistor being driven into saturation and/or cutoff.
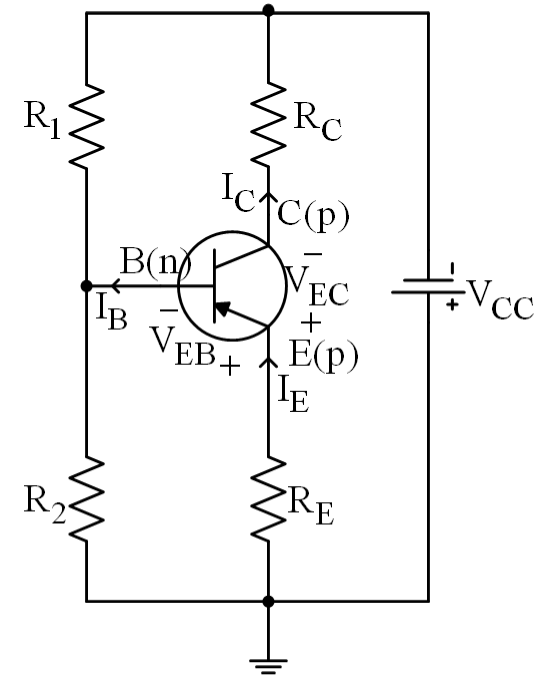
DC BIASING CIRCUITS

1. **Fixed-current/Base biasing circuit - Unstable**
2. **Collector-Base/Collector feedback biasing circuit - Stable**
3. **Voltage division biasing circuit - Stable and the most popular**
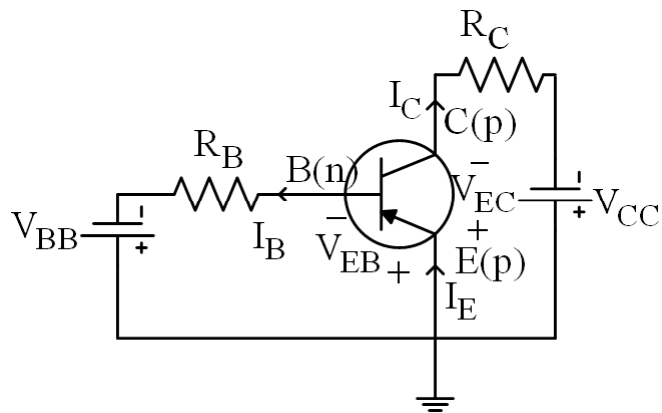
1. Fixed-current/Base biasing circuit

2. Collector to Base /Collector feedback biasing circuit

3. Voltage division biasing circuit

FIXED-CURRENT / BASE BIASING CIRCUIT

KVL for loop I:

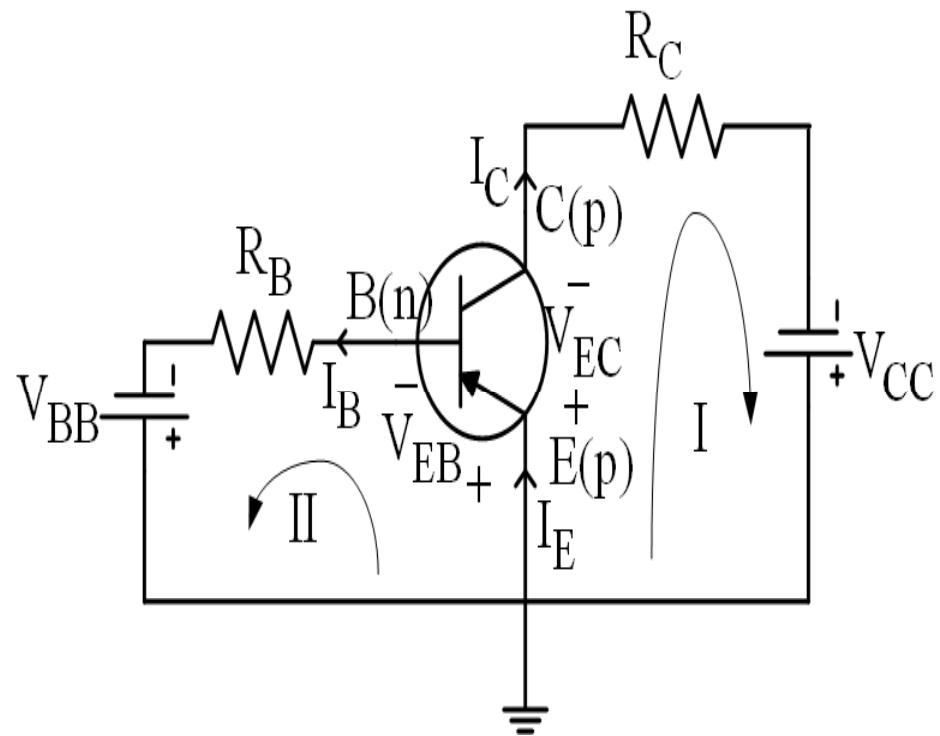$$V_{EC} + I_C R_C - V_{CC} = 0$$
$$V_{EC} + I_C R_C = V_{CC}$$

KVL for loop II:

$$V_{EB} + I_B R_B - V_{BB} = 0$$
$$V_{EB} + I_B R_B = V_{BB}$$
$$I_B = (V_{BB} - V_{EB}) / R_B$$

Since V_{BB} , V_{EB} and R_B are fixed, I_B is also fixed.

COLLECTOR TO BASE / COLLECTOR FEEDBACK BIASING CIRCUIT

KVL of loop I:

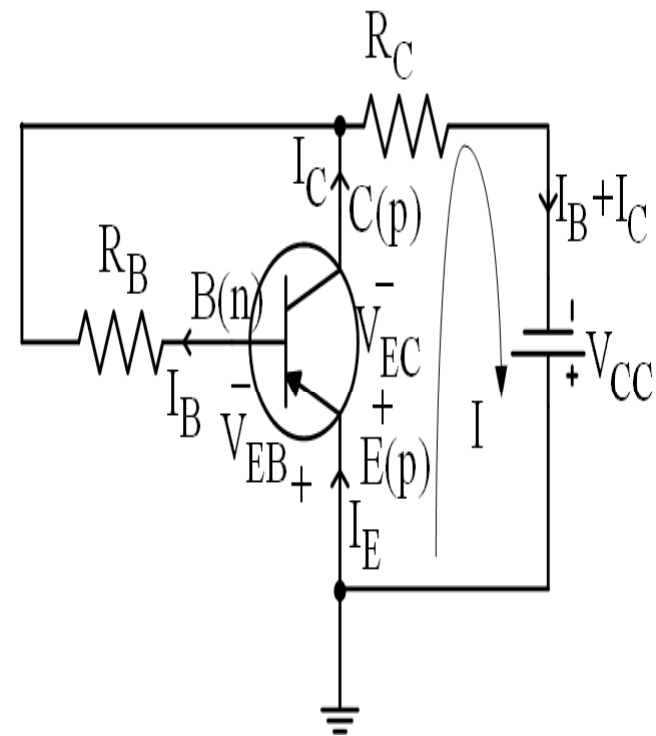$V_{EC} + (I_B + I_C)R_C - V_{CC} = 0$

$V_{EC} + (I_B + I_C)R_C = V_{CC}$

$V_{EC} + (I_B + \beta_{DC}I_B)R_C = V_{CC}$ **if the minority carrier leakage current is neglected.**

KVL of loop II:

$V_{EB} + I_B R_B - V_{EC} = 0$

$I_B = (V_{EC} - V_{EB}) / R_B$

VOLTAGE DIVISION BIASING CIRCUIT

KVL of loop I:

$$I_E R_E + V_{EC} + I_C R_C - V_{CC} = 0$$

KVL of loop II:

$$I_E R_E + V_{EB} + I_B R_T - V_T = 0$$